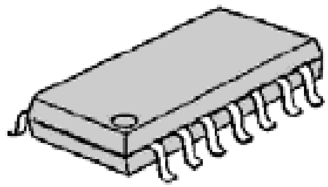
650μA, 9MHz, Rail-to-Rail I/O CMOS Operational Amplifier

DESCRIPTIONS：

The LM334 (quad) is low noise, low voltage, and low power operational amplifier, that can be designed into a wide range of applications. The LM334 have a high gain-bandwidth product of 9MHz, a slew rate of 3.7V/μs, and a quiescent current of 650μA/ amplifier at 5V.



SOP14

The LM334 is designed to provide optimal performance in low voltage and low noise systems. It provides rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5mV for LM334.

It is specified over the extended industrial temperature range (-40℃ to +125℃). The operating range is from 2.5V to 5.5V.

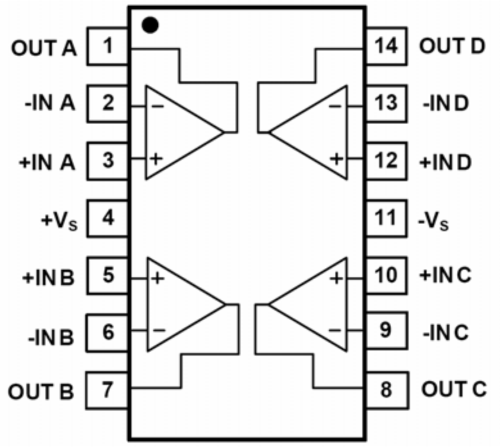
FEATURES

- ◆ Low Cost
- ◆ Rail-to-Rail Input and Output: 0.8m V Typical VOS
- ◆ High Gain- Bandwidth Product: 9 MHz
- ◆ High Slew Rate: 8.0V/μs
- ◆ Settling Time to 0.1% with 2V Step: 1.2μs
- ◆ Overload Recovery Time: 0.4μs
- ◆ Low Noise: 8nV/Hz
- ◆ Operates on 2.5V to 5.5V Supplies
- ◆ Input Voltage Range = -0.1V to + 5.6V with VS = 5.5V
- ◆ Low Power: 650μA/Amplifier Typical Supply Current

APPLICATIONS

- Sensors
- Audio
- Active Filters
- A/D Converters
- Communications
- Test Equipment
- Cellular and Cordless Phones
- Laptops and PDAs
- Photodiode Amplification
- Battery-Powered Instrumentation

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS *1

Characteristic		Value	Unit
Supply Voltage		7.5	V
Common- mode input voltage		(-Vs)-0.5V～(+Vs)+0.5V	V
Operating Temperature		-55 ～+150	℃
Storage Temperature		-65 ～+150	℃
Junction temperature		160	℃
Lead temperature range (soldering 10sec)		260	℃
ESD susceptibility	HBM	1500	V
	MM	400	V

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

(unless otherwise specified: $V_{CM} = V_S/2$, R_L =600Ω, T_A =25℃)

PARAMETER	CONDITION	TYP	MIN/MAX OVER TEMPERATURE					
		+25℃	+25℃	0℃ to 70℃	-40℃ to 85℃	-40℃ to 125℃	UNITS	MIN/ MAX
INPUT CHARACTERISTICS								
Input Offset Voltage (V_{OS})		1	4	4.5	4.75	5	mV	MAX
Input Bias Current (I_B)		1					pA	TYP
Input Offset Current (I_{OS})		1					pA	TYP
Common-Mode Voltage Range (V_{CM})	V_S = 5.5V	-0.1 to +5.6					V	TYP
Common-Mode Rejection Ratio(CMRR)	V_S = 5.5V, V_{CM} = - 0.1V to 4 V	91	75	74	73	72.5	dB	MIN
	V_S = 5.5V, V_{CM} = - 0.1V to 5.6 V	86	64	64	63	62	dB	MIN
Open-Loop Voltage Gain(A_{OL})	R_L = 600Ω ,Vo = 0.15V to 4.85V	90	84	81	80	72	dB	MIN
	R_L =10KΩ ,Vo = 0.05V to 4.95V	100	95	90	88	77	dB	MIN
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta_T$)		2.1					μV/℃	TYP
OUTPUT CHARACTERISTICS								
Output Voltage Swing from Rail	R_L = 600Ω	0.1					V	TYP
	R_L = 10KΩ	0.015					V	TYP
Output Current (I_{OUT})		57	53	52	50	45	mA	MIN
Closed-Loop Output Impedance	F = 1MHz, G = +1	5.7					Ω	TYP
POWER-DOWN DISABLE								
Turn-On Time		2.2					μs	TYP
Turn-Off Time		0.8					μs	TYP
$\overline{DISABLE}$ Voltage-Off			0.8				V	MAX
$\overline{DISABLE}$ Voltage-On			2				V	MIN
POWER SUPPLY								
Operating Voltage Range			2.5	2.5	2.5	2.5	V	MIN
			5.5	5.5	5.5	5.5	V	MAX
Power Supply Rejection Ratio (PSRR)	V_s = +2.5 V to + 5.5 V							
	V_{CM} = $(-V_S)$ + 0.5V	100	80	79	78	77	dB	MIN
Quiescent Current/ Amplifier (I_Q)	I_{OUT} = 0	0.65	0.8	0.9	0.92	1.02	mA	MAX
Supply Current when Disabled								
		0.16	1				μA	MAX
DYNAMIC PERFORMANCE	R_L = 600Ω							
Gain-Bandwidth Product (GBP)		9.0					MHz	TYP
Phase Margin(φ_O)		63.5					degrees	TYP
Full Power Bandwidth(BW_P)	＜1% distortion	400					KHz	TYP
Slew Rate (SR)	G = +1, 2 V Output Step	8.0					V/μs	TYP
Settling Time to 0.1%(t_S)	G = +1, 2 V Output Step	0.36					μs	TYP
Overload Recovery Time	V_{IN} ·Gain = Vs	0.4					μs	TYP
NOISE PERFORMANCE								
Voltage Noise Density (e_n)	f = 1kHz	8					$nV/\sqrt{Hz}$	TYP
	f = 10kHz	6.4					$nV/\sqrt{Hz}$	TYP
Current Noise Density(i_n)	f = 1kHz	10					$fA/\sqrt{Hz}$	TYP

APPLICATION SUMMARY

Driving Capacitive Loads

The LM334 can directly drive 1000pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation.

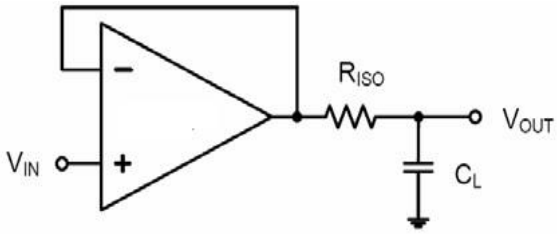


Figure 1. Indirectly Driving Heavy Capacitive Load

Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1.
The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

An improvement circuit is shown in Figure 2.
It provides DC accuracy as well as AC stability. RF provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

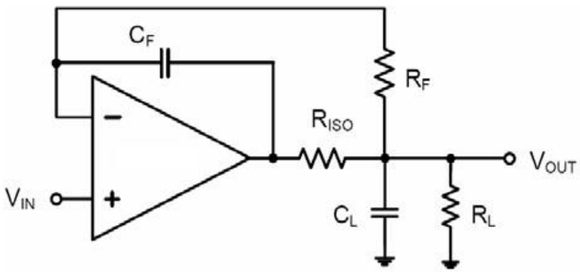


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The LM334 family operates from either a single +2.5 V to +5.5V supply or dual ±1.25V to ±2.75V supplies. For single-supply operation, bypass the power supply V_{DD} with a 0.1µF ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 0.1µF ceramic capacitors. 2.2µF tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

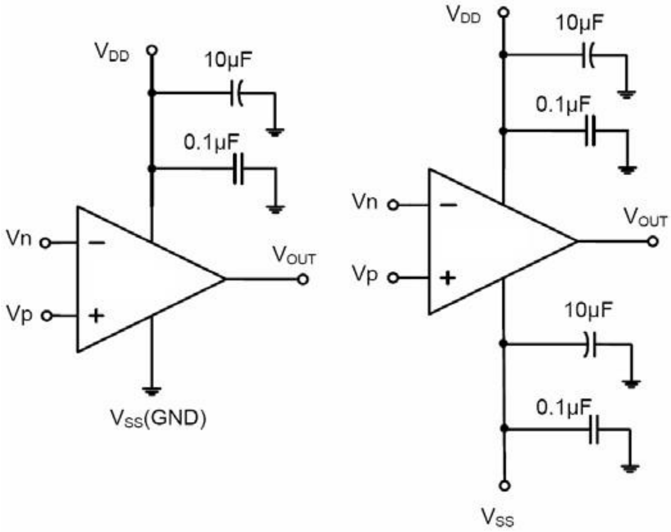


Figure 3. Amplifier with Bypass Capacitors Grounding

Grounding

A ground plane layer is important for LM334circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistors ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (Vp - Vn) \times R_2/R_1 + V_{REF}$.

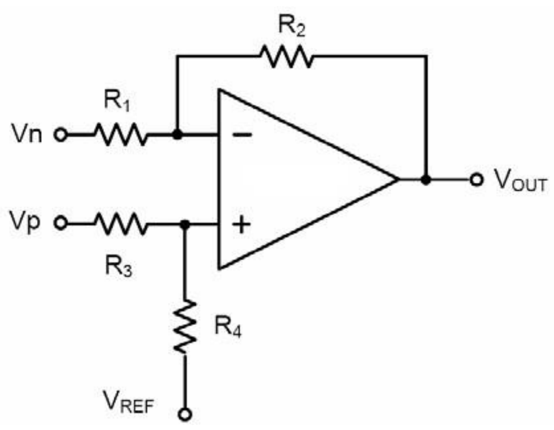


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

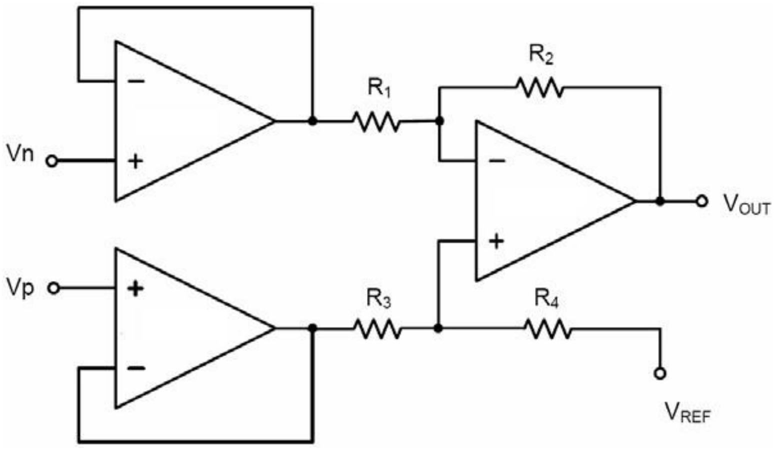


Figure 5. Instrumentation Amplifier Low Pass Active Filter

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of $(-R_2/R_1)$ and the –3dB corner frequency is $1/2\pi R_2C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

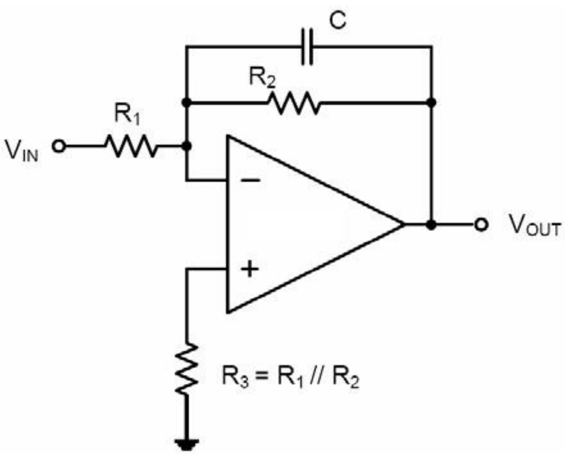
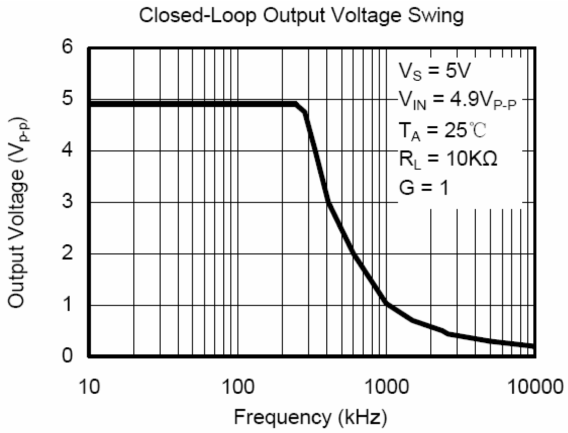
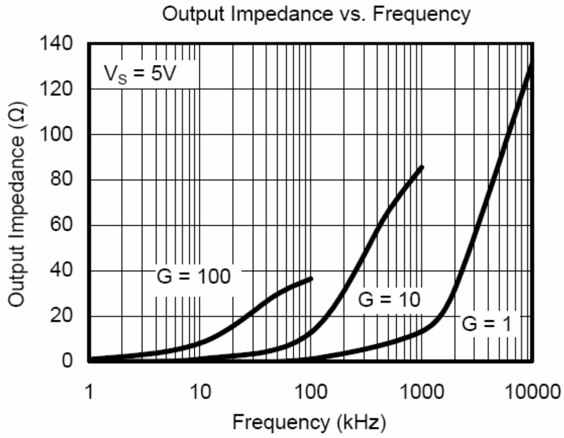


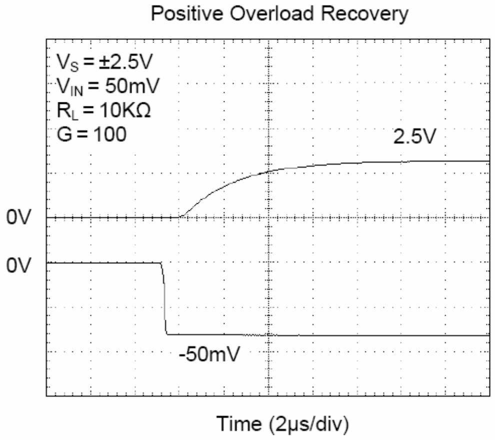
Figure 6. Low Pass Active Filter

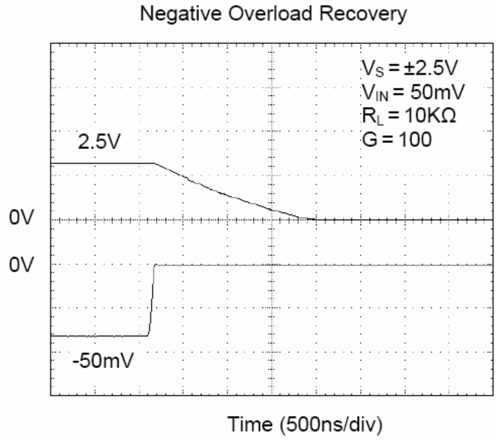
TYPICAL CURVE

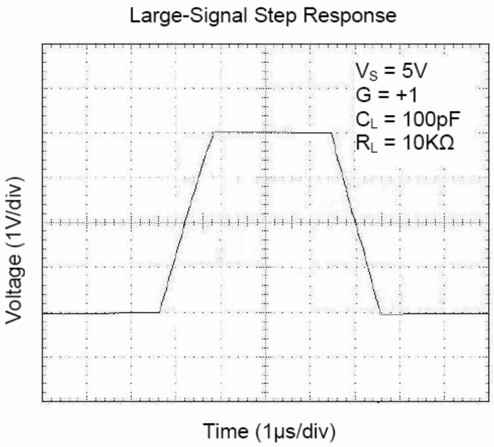
(At TA =25℃, VCM = VS /2, RL =600Ω, unless otherwise noted)

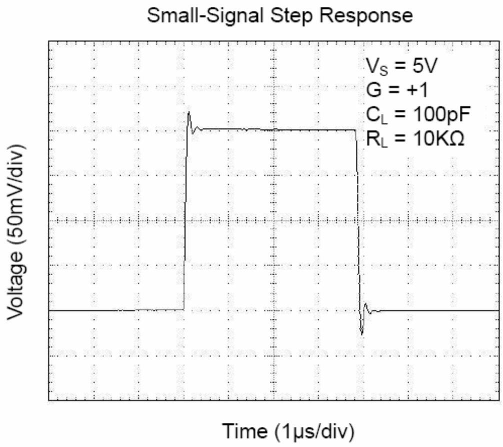


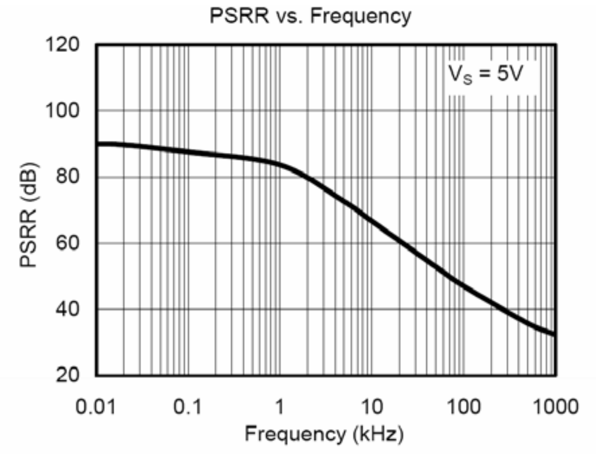


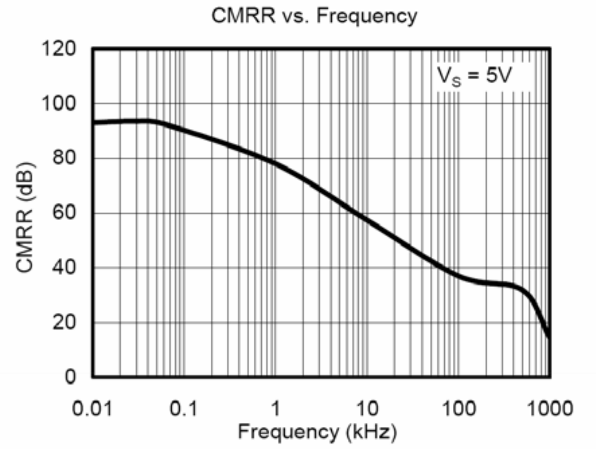


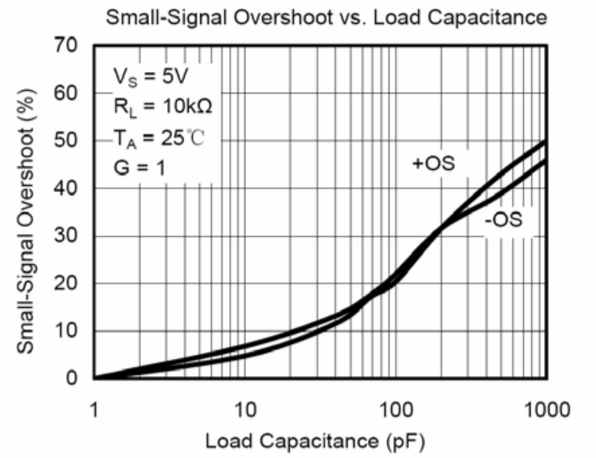


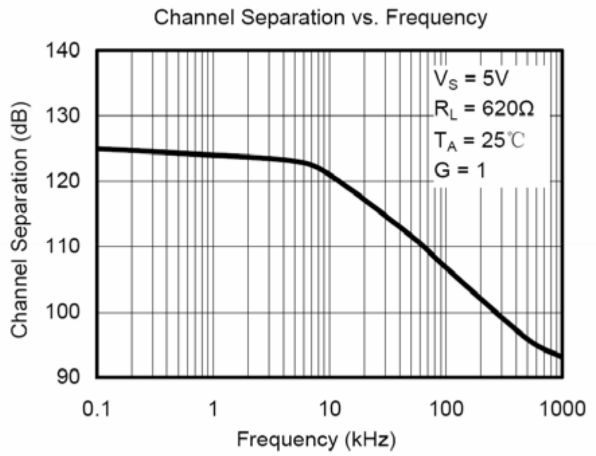


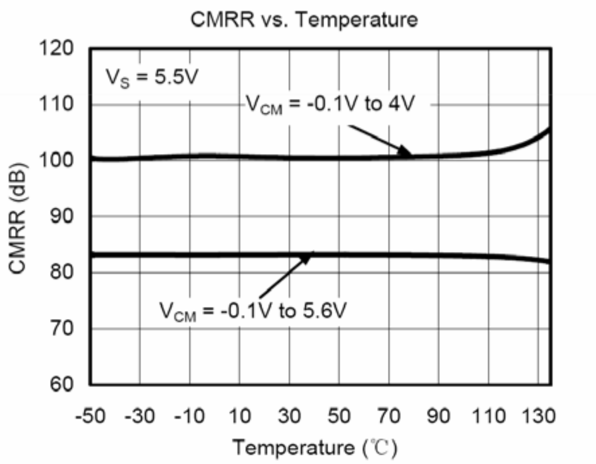


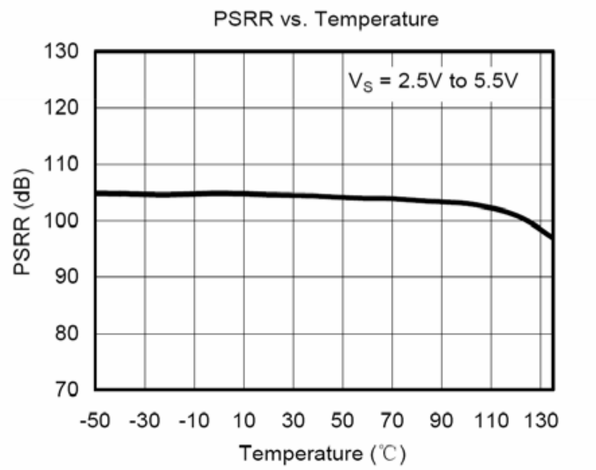

PSRR vs. Frequency
VS = 5V
PSRR (dB)
120
100
80
60
40
20
0.01
0.1
1
10
100
1000
Frequency (kHz)

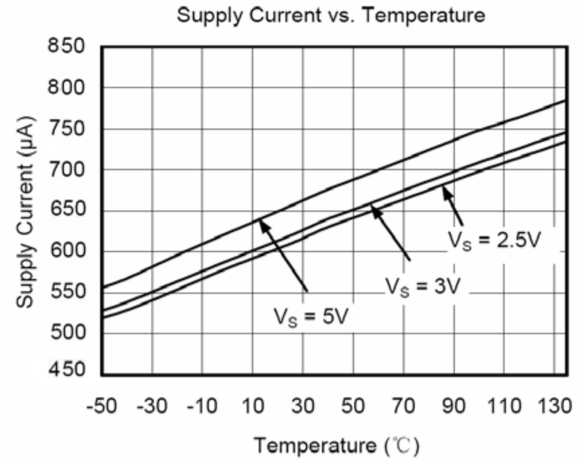

CMRR vs. Frequency
VS = 5V
CMRR (dB)
120
100
80
60
40
20
0
0.01
0.1
1
10
100
1000
Frequency (kHz)


Small-Signal Overshoot vs. Load Capacitance
VS = 5V
RL = 10kΩ
TA = 25℃
G = 1
+OS
-OS
Small-Signal Overshoot (%)
70
60
50
40
30
20
10
0
1
10
100
1000
Load Capacitance (pF)

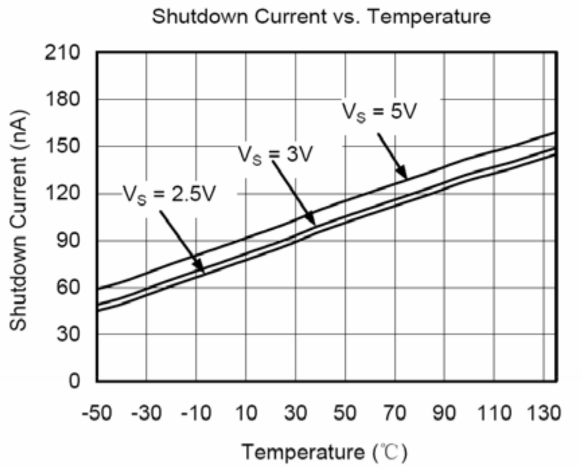

Channel Separation vs. Frequency
VS = 5V
RL = 620Ω
TA = 25℃
G = 1
Channel Separation (dB)
140
130
120
110
100
90
0.1
1
10
100
1000
Frequency (kHz)


CMRR vs. Temperature
VS = 5.5V
VCM = -0.1V to 4V
VCM = -0.1V to 5.6V
CMRR (dB)
120
110
100
90
80
70
60
-50
-30
-10
10
30
50
70
90
110
130
Temperature (℃)

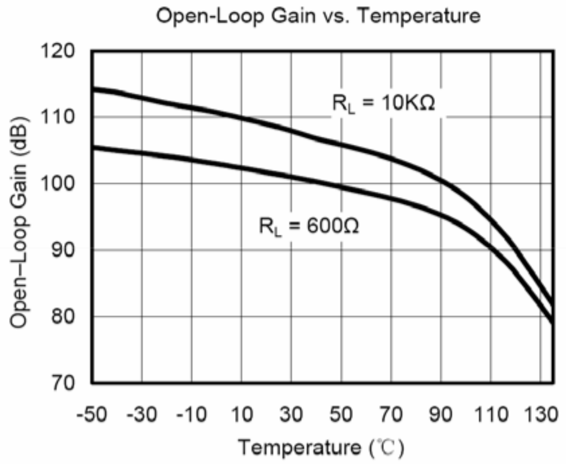

PSRR vs. Temperature
VS = 2.5V to 5.5V
PSRR (dB)
130
120
110
100
90
80
70
-50
-30
-10
10
30
50
70
90
110
130
Temperature (℃)



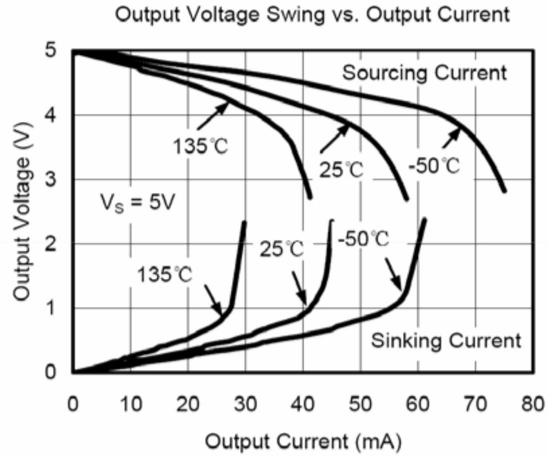
Supply Current vs. Temperature
Supply Current (μA)
Temperature (℃)
V_S = 5V
V_S = 3V
V_S = 2.5V



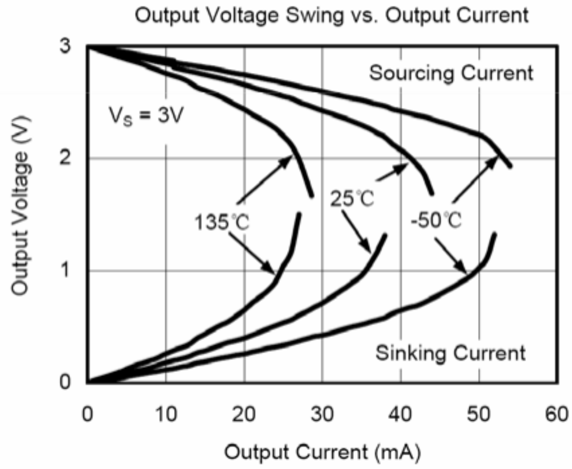
Shutdown Current vs. Temperature
Shutdown Current (nA)
Temperature (℃)
V_S = 5V
V_S = 3V
V_S = 2.5V



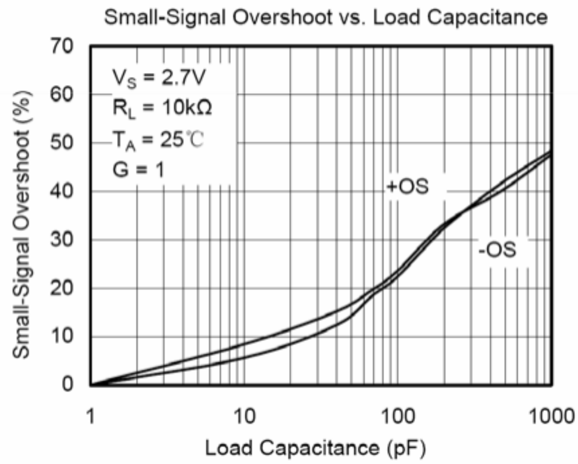
Open-Loop Gain vs. Temperature
Open–Loop Gain (dB)
Temperature (℃)
R_L = 10KΩ
R_L = 600Ω



Output Voltage Swing vs. Output Current
Output Voltage (V)
Output Current (mA)
Sourcing Current
Sinking Current
V_S = 5V
135℃
25℃
-50℃

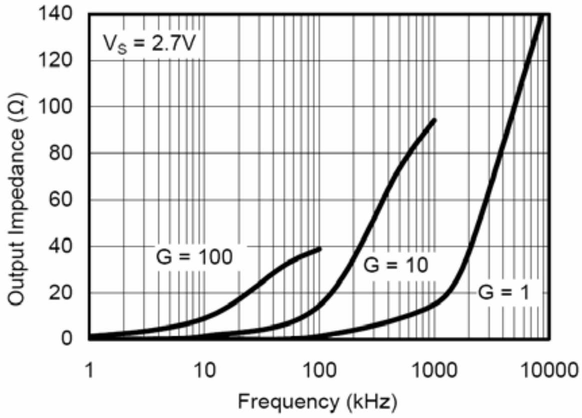


Output Voltage Swing vs. Output Current
Output Voltage (V)
Output Current (mA)
Sourcing Current
Sinking Current
V_S = 3V
135℃
25℃
-50℃

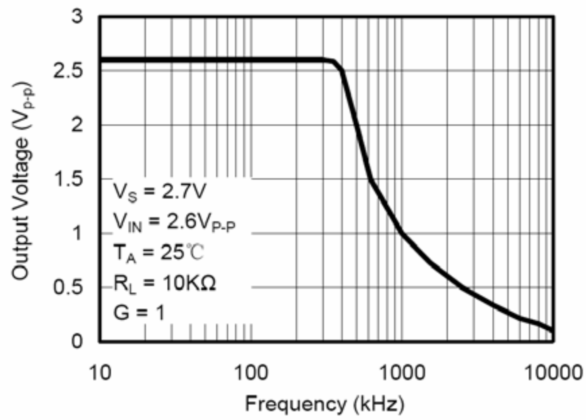


Small-Signal Overshoot vs. Load Capacitance
Small-Signal Overshoot (%)
Load Capacitance (pF)
V_S = 2.7V
R_L = 10kΩ
T_A = 25℃
G = 1
+OS
-OS

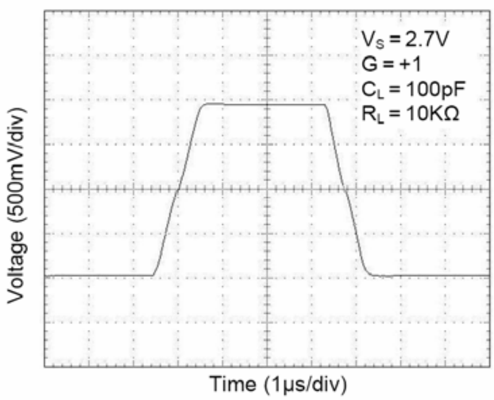
Output Impedance vs. Frequency



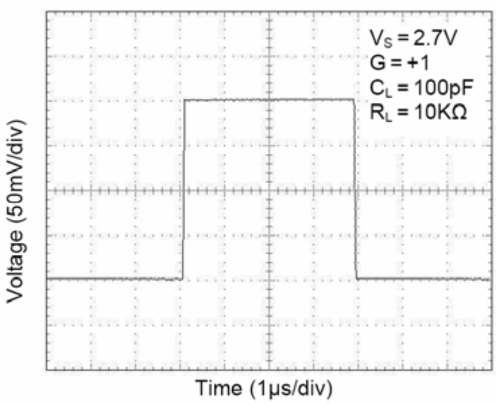
Closed-Loop Output Voltage Swing



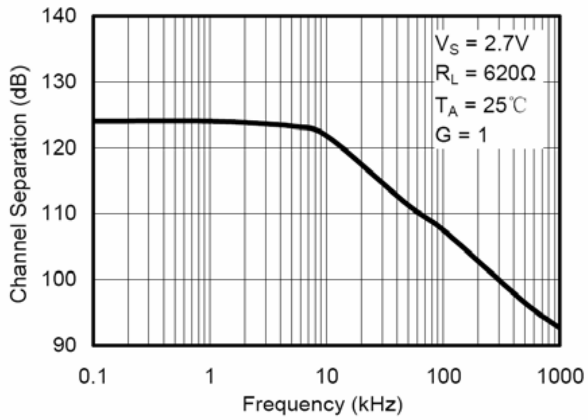
Large-Signal Step Response



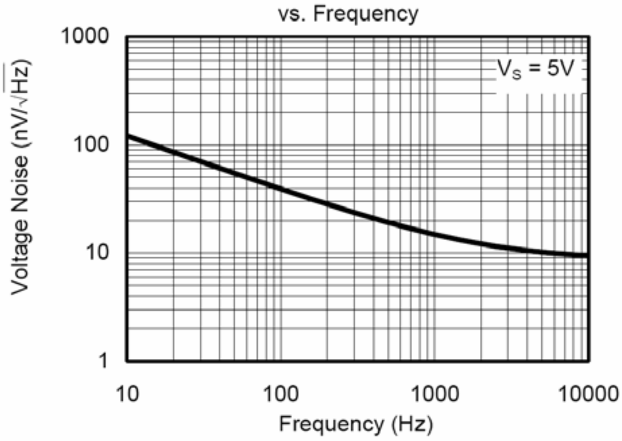
Small-Signal Step Response



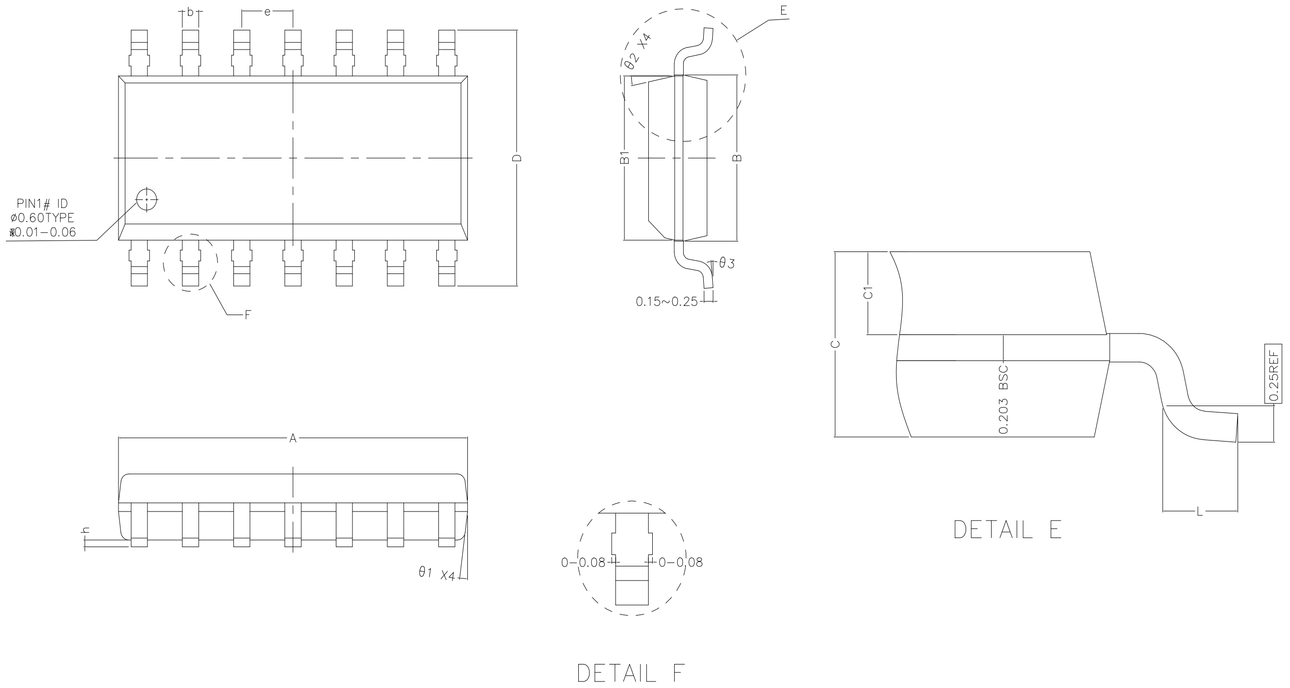
Channel Separation vs. Frequency



Input Voltage Noise Spectral Density vs. Frequency



OUTLINE DRAWING



COMMON DIMENSIONS (UNITS OF MEASURE IS mm)			
	MIN	NORMAL	MAX
A	8.500	8.600	8.700
B	3.800	3.900	4.000
B1	3.750	3.850	3.950
C	1.300	1.400	1.500
C1	0.600	0.650	0.700
D	5.800	6.000	6.200
L	0.450	0.600	0.750
b	0.350	0.400	0.450
h	0.050	0.100	0.250
e	1.270TYPE		
θ_1	12° TYPE		
θ_2	12° TYPE		
θ_3	0° ~ 8°		